International Journal of Current Research and Modern Education (IJCRME)
ISSN (Online): 2455 – 5428 & Impact Factor: 3.165
Special Issue, NCFTCCPS - 2016

POWER REDUCTION IN FULL ADDER USING NEW HYBRID LOGIC

V. Kayathri*, C. Kumar, P. Mari Muthu*****
& N. Naveen Kumar****
Department of Electronics and Communication Engineering, RVS College of Engineering and Technology, Coimbatore, Tamilnadu

Abstract:

*In this paper, a full adder circuit is designed by using new hybrid logic. Complementary metal oxide semiconductor logic and transmission gate logic is combined to produce a hybrid logic. This proposed full adder design contains 3 modules. Module 1 and module 2 generates the sum output of the adder circuit. Module 3 generates the carry output of the circuit. Simulation process is done in tanner tool at 180nm technology. Proposed adder design is compared to the previous hybrid adder circuit (5.74*10^-2), then the power of the proposed full adder design is (2.60*10^-2) less.*

Index Terms: Carry Propagation Adder, High Speed & Hybrid Design and Low Power.

Introduction:

Historically, the earliest and the most pressing demands for low power came from portable devices such as pocket calculators and laptops. These products have always put a large emphasis on minimizing power in order to maximize battery life .The prolific growth of portable battery energized electronics with high throughput such as laptops, personal digital assistants (PDA's), cellular phones and pagers has placed power as pivotal design constraint possibly out placing speed and area in some cases .However as predicted by Moore's law, the number of transistors per chip has been increasing by about 1.5 times per year.

The full adder circuit is an important building block of digital arithmetic circuits. Its purpose is to form the arithmetic sum of two binary numbers. Microprocessors and digital signal processors rely on the efficient implementation of generic arithmetic units to execute complicated algorithms like filtering, FFT. In these applications, multipliers are an important dissipation source. The basic element in multiplier is adder circuit so Therefore, power-efficient multipliers require power efficient implementation of adder circuit.

$$SUM=A \oplus B \oplus CIN$$
$$COUT=A.B+B.CIN+A.CIN$$

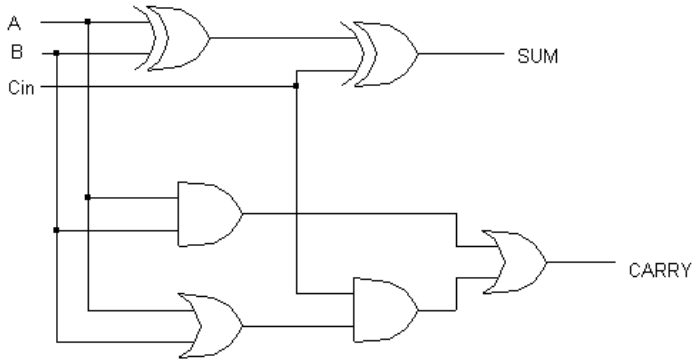


Figure 1: Schematic diagram of the basic full adder circuit using logic gates

A and **B** are the bits to be added, **CIN** is the carry bit generated by the previous bit position, **SUM** is the sum bit for the current bit position, and **COUT** is the carry

generated in the current bit position. A device for summing three bits in this manner is called *a full adder.*

In this paper different logic styles are compared to minimize the power consumption in full adder circuit. Complementary metal oxide semiconductor logic, complementary pass-transistor logic (CPL), Transmission gate full adder (TGA) and hybrid logic style are the most important logic design styles in the conventional domain. The other adder designs use more than one logic style, known as hybrid-logic design style, for their implementation. These designs exploit the features of different logic styles to improve the overall performance of the full adder. Pass transistor logic is one of the well-known MOS logic style used to implement different functions. General method for deriving pass transistor logic diagram for a function is choosing control variable and pass variable based on the functional description. The advantages of pass transistor logic are it operates full swing and area is reduced due to less moss transistors, disadvantage is more delay in long chain of operation. Transmission gate approach is another widely used CMOS design style to implement digital function. Transmission gate based implementation is similar to pass transistor with the difference that transmission gate logic uses nMOS and pMOS transistors. Its advantage is conduct both strong 0 and strong 1, disadvantage is chip area is increased .The advantages of standard complementary (CMOS) style-based adders (with 28 transistors) are its robustness against voltage scaling and transistor sizing; while the disadvantages are high input capacitance and requirement of buffers.

Design of the Existing Full Adders:

A. CMOS Logic Full Adder:

CMOS circuits use a combination of p-type and n-type metal–oxide–semiconductor field-effect transistor (MOSFETs) to implement logic gatesand other digital circuits. In this implementation 28 transistors are used to design the circuit

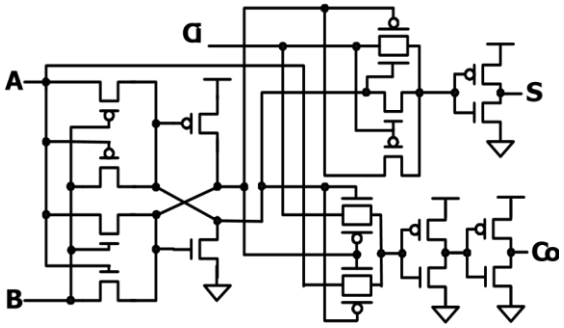


Figure 2: Circuit diagram for CMOS logic full adder

B. Pass Transistor Logic:

It reduces the count of transistors used to make different logic gates, by eliminating redundant transistors. Transistors are used as switches to pass logic levels between nodes of a circuit, instead of as switches connected directly to supply voltages.[1] This reduces the number of active devices, but has the disadvantage that the difference of the voltage between high and low logic levels decreases at each stage. Each transistor in series is less saturated at its output than at its input. If several devices are chained in series in a logic path, a conventionally constructed gate may be required to restore the signal voltage to the full value. By contrast, conventional CMOS logic switches transistors so the output connects to one of the power supply rails, so logic voltage levels in a sequential chain do not decrease. Simulation of circuits may be required to ensure adequate performance.

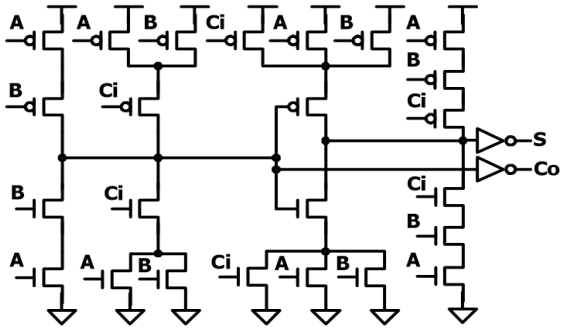


Figure 3 circuit diagram of a full adder using pass transistor logic C. Transmission Gate Logic In principle, a transmission gate made up of two field effect transistors, in which - in contrast to traditional discrete field effect transistors - the substrate terminal (Bulk) is not connected internally to the source terminal. The two transistors, an n-channel MOSFET and a p-channel MOSFET are connected in parallel with this, however, only the drain and source terminals of the two transistors are connected together.

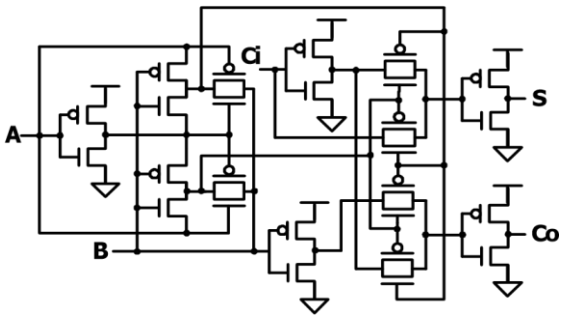


Figure 4 circuit diagram of a full adder using transmission gate logic D. Hybrid logic In hybrid logic two or more logics are combined to design a circuit. In this circuit complementary pass transistor logic and transmission gate logic is combined to design the full adder .totally 16 transistors are used to design the full adder .The advantage of this method is power consumption is reduced, disadvantage is more delay is occurred when the one bit adder is connected in cascaded form to extend 16 bit adder.

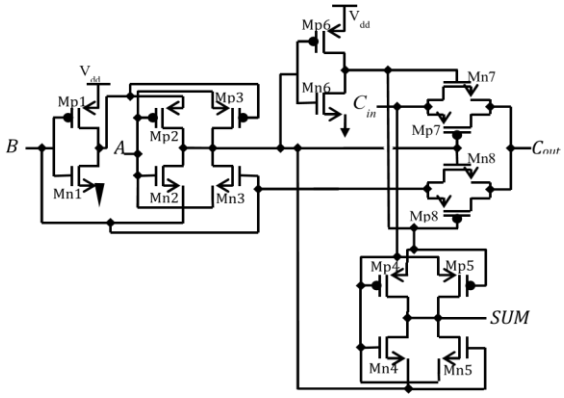


Figure 5: Circuit diagram of the hybrid full adder

Simulation Results:

Simulation is done by using tanner software tool at 180 nm technology. Input supply voltage is 5v. In this tool the total power consumption of the circuit is analysed and the output waveforms are obtained. The simulation result of full adder using four different logics is given below. Each logic design have its own advantages and disadvantages.

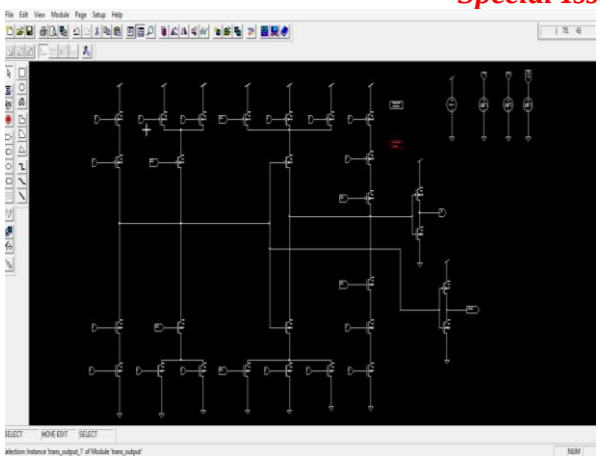


Figure 6: Schematic diagram for full adder using CMOS logic

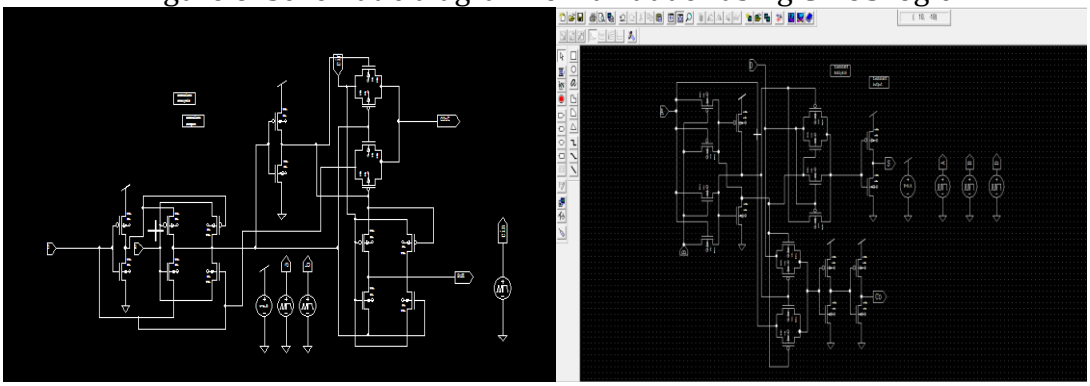


Figure 7: Schematic diagram of full adder using pass transistor logic
Figure 8: Schematic diagram of full adder using transmission gate logic

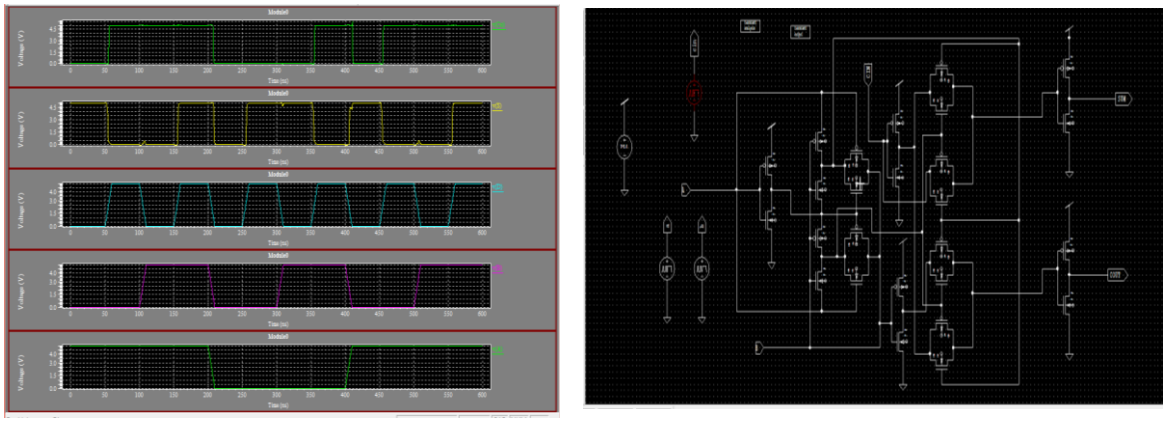
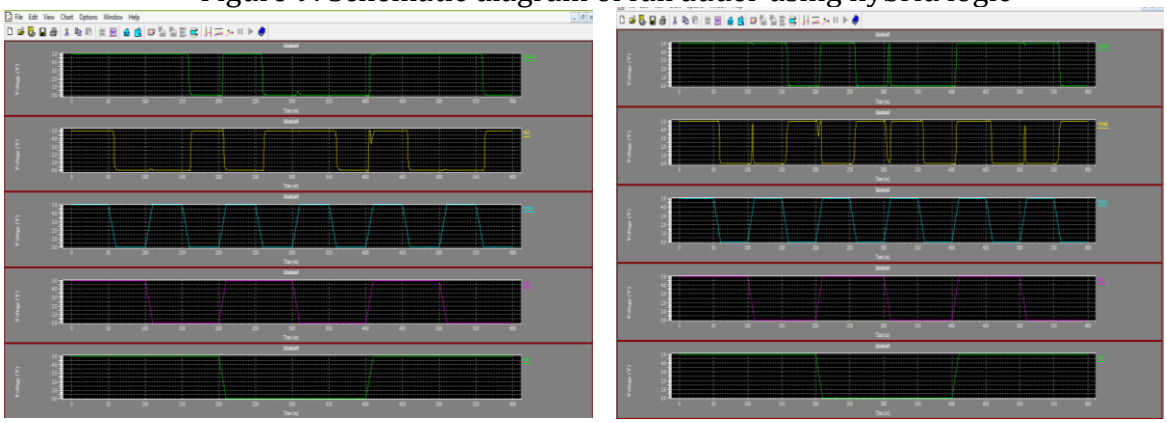


Figure 9: Schematic diagram of full adder using hybrid logic



Output Waveforms:

Output waveform for hybrid logic

Proposed Method:

Existing Full Adder Design Based on Hybrid Logic:

In this existing method, a low-power full adder design using complementary metal oxide transistor logic and transmission gate logic was presented. In full adder designing there are 3 modules are used to produce the output.Module1 and module2 are the xnor modules it generate the sum of the adder circuit. Module 3 generates the carry output of this circuit. Each module are designed individually and connected to produce the sum and carry output of the full adder circuit.

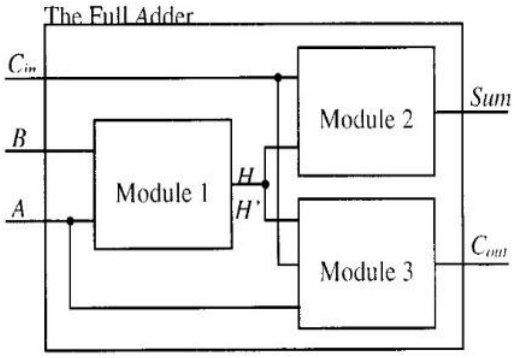


Fig 10: Basic full adder circuit

Module 1:

The first module is able to produce both XOR and XNOR gate outputs. Five different styles are used to design the xnor and xor circuit. XNOR function is obtained by using inverter at the output of the XOR function. Another option is generating both functions simultaneously but it requires more transistors. So the first method is more compact compared to second method .fig a-c follows the first method then fig d and e follows the second method. Figure 4.2 five different designs of XNOR module

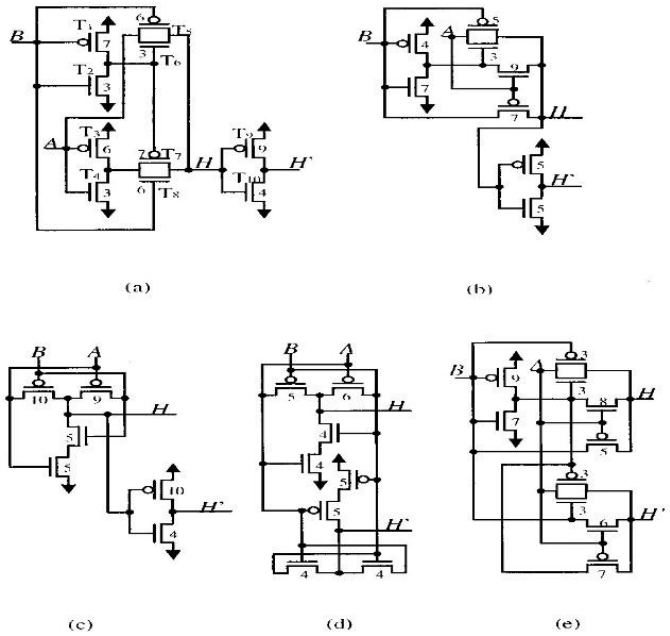


Figure 11: Different design styles of XNOR and XOR module

Fig (a) is composed two transmission gates and three inverters. Fig (b) is composed eight transistors and based on transmission function theory. Fig (c) is composed by 14

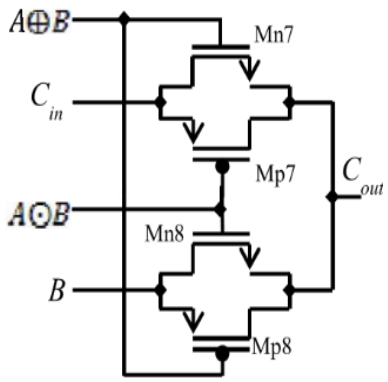
transistors. Fig (d) is composed by eight transistors it uses the same xor function. Fig (e) is composed by using 10 transistors.

Module 2:

Module 2 is combined to module 1 to produce the sum output of the full adder circuit.

Module 3:

It generates the carry output of the full adder circuit.



(c)

Figure 12: Carry Generation Module

The input carry signal propagates to the first transmission gate it reducing the overall carry propagating path.

Proposed Full Adder:

In proposed full adder the number of transistor count is reduced by replacing module 1in the existing full adder circuit. in existing module there is eight transistors are used in the 1 module (XNOR and XOR) this module is replaced by new XNOR module. In this proposed approach the dynamic power dissipation is more concentrated because dynamic power is primary source of the power dissipation. Switching activity is one of the sources in dynamic power dissipation. Switching activity is the probability that the transistor changes from OFF to ON because that is the only time the circuit consumes power. When the transistor count is reduced switching activity of the circuit is also reduced. This strategy is followed by the proposed full adder design.

$$P_{dynamic}=\alpha \times C \times V_{dd}^2 \times f_{sw}$$

Where, α=activity factor
C = Physical Capacitance
f_{sw} = Switching Frequency
V_{dd}^2 = Supply Voltage

Simulation Results:

Simulation is done by using tanner software tool at 180 nm technology. Input supply voltage is 5v. In this tool the total power consumption of the circuit is analysed and the output waveforms are obtained. The simulation result of full adder using hybrid logic style is given below.

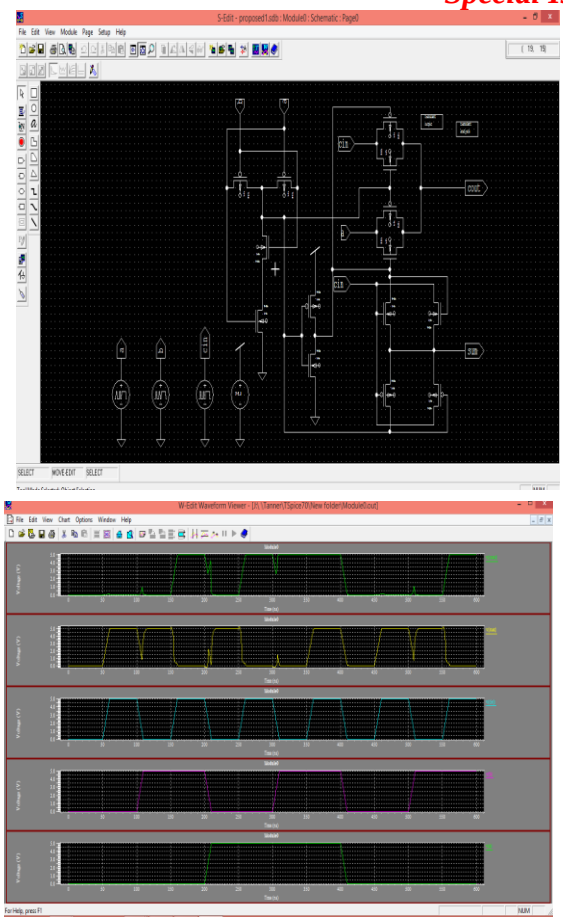


Figure 13: Schematic diagram of the proposed full adder

Comparison Table:

S.No	Name of the Logic	Number of Transistors	Power in Watts
1	CMOS logic	28	$3.7534*10^{-2}$
2	Pass transistor logic	20	$3.4671*10^{-2}$
3	Transmission gate logic	26	$4.2047*10^{-2}$
4	Hybrid logic	16	$5.74*10^{-2}$
5	Proposed adder	14	$2.60*10^{-2}$

Conclusion:

In this project, thus the Hybrid full adder design was presented by employing both CMOS and a transmission gate logic. The power consumption of the circuit is compared against four previous designs. The compared results show that the performance of the proposed design is superior to other reference designs .The key idea was to reduce the number of transistors in the discharging path to enhance both power and area. The design was achieved by hybrid logic. Proposed adder design is compared to the previous hybrid adder circuit (5.74*10^-2), then the power of the proposed full adder design is (2.60*10^-2) less.

References:

1. C.-K. Tung, Y.-C. Hung, S.-H. Shieh, and G.-S. Huang, “A low-power high-speed hybrid CMOS full adder for embedded system,” in Proc. IEEE Conf. Design Diagnostics Electron. Circuits Syst., vol. 13. Apr. 2007, pp. 1–4.

2. S. Goel, A. Kumar, and M. A. Bayoumi, "Design of robust, energyefficient full adders for deep-submicrometer design using hybrid-CMOS logic style," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 14, no. 12, pp. 1309–1321, Dec. 2006.
3. N. H. E. Weste, D. Harris, and A. Banerjee, CMOS VLSI Design: A Circuits and Systems Perspective, 3rd ed. Delhi, India: Pearson Education, 2006.
4. J. M. Rabaey, A. Chandrakasan, and B. Nikolic, Digital Integrated Circuits: A Design Perspective, 2nd ed. Delhi, India: Pearson Education, 2003.
5. D. Radhakrishnan, "Low-voltage low-power CMOS full adder," IEE Proc.-Circuits Devices Syst., vol. 148, no. 1, pp. 19–24, Feb. 2001.
6. C. H. Chang, J. M. Gu, and M. Zhang, "A review of 0.18-μm full adder performances for tree structured arithmetic circuits," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 13, no. 6, pp. 686–695, Jun. 2005.
7. A. M. Shams, T. K. Darwish, and M. A. Bayoumi, "Performance analysis of low-power 1-bit CMOS full adder cells," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 10, no. 1, pp. 20–29, Feb. 2002.
8. M. L. Aranda, R. Báez, and O. G. Diaz, "Hybrid adders for high-speed arithmetic circuits: A comparison," in Proc. 7th IEEE Int. Conf. Elect. Eng. Comput. Sci. Autom. Control (CCE), Tuxtla Gutierrez, NM, USA, Sep. 2010, pp. 546–549.
9. M. Vesterbacka, "A 14-transistor CMOS full adder with full voltageswing nodes," in Proc. IEEE Workshop Signal Process. Syst. (SiPS), Taipei, Taiwan, Oct. 1999, pp. 713–722.
10. M. Zhang, J. Gu, and C.-H. Chang, "A novel hybrid pass logic with static CMOS output drive full-adder cell," in Proc. Int. Symp. Circuits Syst., May 2003, pp. 317–320.
11. S. Wairya, G. Singh, R. K. Nagaria, and S. Tiwari, "Design analysis of XOR (4T) based low voltage CMOS full adder circuit," in Proc. IEEE Nirma Univ. Int. Conf. Eng. (NUiCONE), Dec. 2011, pp. 1–7.
12. S. Goel, M. Elgamel, and M. A. Bayoumi, "Novel design methodology for high-performance XOR-XNOR circuit design," in Proc. 16th Symp.
Integr. Circuits Syst. Design (SBCCI), Sep. 2003, pp. 71–76.
13. J.-M. Wang, S.-C. Fang, and W.-S. Feng, "New efficient designs for XOR and XNOR functions on the transistor level," IEEE J. Solid-State Circuits, vol. 29, no. 7, pp. 780–786, Jul. 1994.
14. P. Prashanth and P. Swamy, "Architecture of adders based on speed, area and power dissipation," in Proc. World Congr. Inf. Commun. Technol. (WICT), Dec. 2011, pp. 240–244.
15. M. J. Zavarei, M. R. Baghbanmanesh, E. Kargaran, H. Nabovati, and A. Golmakani, "Design of new full adder cell using hybrid-CMOS logic style," in Proc. 18th IEEE Int. Conf. Electron., Circuits Syst. (ICECS), Dec. 2011, pp. 451–454.
16. I. Hassoune, D. Flandre, I. O'Connor, and J. Legat, "ULPFA: A new efficient design of a power-aware full adder," IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 57, no. 8, pp. 2066–2074, Aug. 2010.
17. K. Navi, M. Maeen, V. Foroutan, S. Timarchi, and O. Kavehei, "A novel low-power full-adder cell for low voltage," VLSI J. Integr., vol. 42, no. 4, pp. 457–467, Sep. 2009.
18. M. Aguirre-Hernandez and M. Linares-Aranda, "CMOS full-adders for energy-efficient arithmetic applications," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 19, no. 4, pp. 718–721, Apr. 2011.
19. J. L. Wyatt, Jr., "Signal propagation delay in RC models for interconnect," in Circuit Analysis, Simulation and Design, Part II, VLSI Circuit Analysis and Simulation, vol. 3, A. Ruehli, Ed. Amsterdam, The Netherlands: North Holland, 1987, ch. 11.

20. M. Alioto, G. Di Cataldo, and G. Palumbo, "Mixed full adder topologies for high-performance low-power arithmetic circuits," Microelectron. J., vol. 38, no. 1, pp. 130–139, Jan. 2007.
21. X. Wu and F. Prosser, "Design of ternary CMOS circuits based on transmission function theory," Int. J. Electron., vol. 65, no. 5, pp. 891–905, 1988.
22. K. Navi, M. H. Moaiyeri, R. F. Mirzaee, O. Hashemipour, and B. M. Nezhad, "Two new low-power full adders based on majority-not gates," Microelectron. J., vol. 40, no. 1, pp. 126–130, Jan. 2009.
23. H. T. Bui, Y. Wang, and Y. Jiang, "Design and analysis of low-power 10-transistor full adders using novel XOR-XNOR gates," IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process., vol. 49, no. 1, pp. 25–30, Jan. 2002.
24. K. Naviet al., "A novel low-power full-adder cell with new technique in designing logical gates based on static CMOS inverter," Microelectron. J., vol. 40, no. 10, pp. 1441–1448, Oct. 2009.